AMENDMENTS TO THE CLAIMS

1-19. (Canceled)

20. (Currently Amended) A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first well of an integrated circuit substrate;

forming a protection circuit occupying a second well of the ~~an~~ integrated circuit substrate separate from the first well wherein forming a protection circuit includes forming a unit diode, the unit diode comprised of a block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region, a junction region of the integrated circuit substrate surrounding the doped region, and a contact to the doped region, the doped region being a first doped region of a first dopant in the second well of the substrate, the second well being doped with a first concentration of a second dopant and the junction region separating the first doped region from the second well, wherein forming a protection circuit includes forming a third doped region in the second well adjacent the junction region, the third doped region doped with a second concentration of the second dopant; and

coupling the protection circuit to the performance circuit.

21. (Previously Presented) The method of claim 20, wherein forming a performance circuit includes forming a CMOS configuration.

22. (Previously Presented) The method of claim 21, wherein coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS configuration.

23. (Previously Presented) The method of claim 21, wherein forming a protection circuit includes forming a diode and coupling the protection circuit to the performance circuit includes coupling the diode to a p-channel device of the CMOS configuration.

24-25. (Canceled.)

26. (Currently Amended) The method of claim 20 ~~25~~, wherein forming a protection circuit includes forming a plurality of unit diodes.

27. (Currently Amended) A method of forming an integrated circuit comprising: ~~The method of claim 20, wherein forming a performance circuit includes:~~

forming a performance circuit occupying a first well of an integrated circuit substrate, wherein forming a performance circuit includes:

forming a unit transistor device having a drain region comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the doped region;

forming a gate region of the integrated circuit substrate surrounding the doped region; and

forming a contact to the doped region; ~~.~~

forming a protection circuit occupying a second well of the integrated circuit substrate separate from the first well; and

coupling the protection circuit to the performance circuit.

28. (Previously Presented) The method of claim 27, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a concentration of a second dopant and wherein forming a performance circuit further comprises:

forming a source region of the transistor doped with the first dopant in the well separated from the drain region by the gate to form a unit transistor.

29. (Previously Presented) The method of claim 28, wherein forming a performance circuit includes:

forming a plurality of unit transistors.